AMENDMENTS TO THE CLAIMS

Please amend the claims as shown below:

1(Original). A power conversion integrated circuit, comprising:

a state circuit having an output that supplies a mode signal, wherein the state circuit includes

a comparator having a first input coupled for receiving a control signal and a second input coupled for receiving a first reference signal, and

a memory circuit having a first input coupled to an output of the comparator for setting an output state of the memory circuit according to a value of the control signal; and

a control circuit coupled for receiving the mode signal that sets a mode of operation, where the control circuit is responsive to a feedback signal for providing a pulse-width modulated control signal.

2(Original). The power conversion integrated circuit of claim 1, wherein the comparator includes:

a first comparator having a first input coupled for receiving the control signal, a second input coupled for receiving the first reference signal, and an output coupled to the first input of the memory circuit; and

a second comparator having a first input coupled for receiving the control signal, a second input coupled for receiving a second reference signal, and an output coupled to a second input of the memory circuit.

3(Original). The power conversion integrated circuit of claim 2, further including a resistor divider network for

generating the first reference signal at a first output and the second reference signal at a second output.

4(Original). The power conversion integrated circuit of claim 3, wherein the resistor divider network includes:

a first resistor having first and second terminals, the first terminal of the first resistor coupled to a first power supply conductor;

a second resistor having first and second terminals, the first terminal of the second resistor coupled to the second terminal of the first resistor and serving as the first output of the resistor divider network; and

a third resistor having first and second terminals, the first terminal of the third resistor coupled to the second terminal of the second resistor and serving as the second output of the resistor divider network, and the second terminal of the third resistor coupled to a second power supply conductor.

5(Original). The power conversion integrated circuit of claim 4, further including a pulse filter having an input coupled to the output of the second comparator and an output coupled to the second input of the memory circuit.

6(Original). The power conversion integrated circuit of claim 1, wherein the memory circuit has at least one storage element for storing an operating mode of the power conversion integrated circuit.

7(Original). The power conversion integrated circuit of claim 1, further including a reset circuit having an input coupled to a logic under voltage signal and an output coupled to the control signal.

8(Original). A semiconductor chip having at least four external electrical connections, comprising:

an internal regulator; a state circuit having an output coupled to a control input of the internal regulator;

a first electrical connection terminal for coupling an external ground reference to an internal ground reference of the internal regulator;

a second electrical connection terminal for providing a pulse-width modulated output signal from an output of the internal regulator;

a third electrical connection terminal coupled for receiving a feedback signal at an input of the internal regulator to control the pulse-width modulated output signal; and

a fourth electrical connection terminal coupled for receiving a control signal which is applied to the state circuit to set a mode of operation of the internal regulator.

9(Original). The semiconductor chip of claim 8, further comprising a fifth electrical connection terminal coupled for receiving a bias voltage which is applied to the state circuit and to the internal regulator.

10(Original). A programmable power supply, comprising:

a transformer receiving a rectified signal at a primary side of the transformer;

a state circuit having an input and an output for setting a mode of operation of the programmable power supply, wherein the state circuit includes,

a comparator circuit having a first input coupled to the input of the state circuit for receiving a control signal and a

second input coupled for receiving a first reference signal, and

a memory circuit having a first input coupled to an output of the comparator for setting an output state of the memory circuit according to a value of the control signal where the output state of the memory circuit controls the mode of operation;

a control circuit coupled for receiving the output state of the memory circuit and wherein the control circuit is responsive to a feedback signal for providing a pulse-width modulated control signal; and

a transistor having a control terminal for receiving the pulse-width modulated control signal, a first conduction terminal coupled to the primary side of the transformer, and a second conduction terminal coupled to ground.

11(Original). The programmable power supply of claim 10, wherein the comparator circuit includes:

a first comparator having a first input coupled for receiving the control signal, a second input coupled for receiving the first reference signal, and an output coupled to the first input of the memory circuit; and

a second comparator having a first input coupled for receiving the control signal, a second input coupled for receiving a second reference signal, and an output coupled to a second input of the memory circuit.

12(Original). The programmable power supply of claim 10, further including a resistor divider network for generating a first reference signal at a first output and a second reference signal at a second output.

13(Original). The programmable power supply of claim 12, wherein the resistor divider network includes:

a first resistor having first and second terminals, the first terminal of the first resistor coupled to a first power supply conductor;

a second resistor having first and second terminals, the first terminal of the second resistor coupled to the second terminal of the first resistor and serving as the first output of the resistor divider network; and

a third resistor having first and second terminals, the first terminal of the third resistor coupled to the second terminal of the second resistor and serving as the second output of the resistor divider network, and the second terminal of the third resistor coupled to a second power supply conductor.

14(Original). A method for controlling a mode of operation of a power converter, comprising the steps of:

controlling a pulse-width modulated output signal of the power converter in response to a feedback signal; and

setting a memory state according to a comparison between a control signal and a first reference signal where the memory state controls the mode of operation of the power converter.

15(Original). The method of claim 14, further comprising the steps of:

monitoring a signal at an input pin; and

maintaining a same operating state when the input pin receives a voltage about midway between an operating potential and a ground reference.

16(Original). The method of claim 14, further comprising the steps of requesting an on-operating state when a power

supply is off and an input pin receives a voltage greater than a first reference voltage.

17(Original). The method of claim 14, further comprising the steps of requesting a toggle condition when a power supply is on and an input pin receives a voltage greater than a first reference voltage.

18(Original). The method of claim 15, further comprising the steps of requesting that an output state be toggled when a power supply is on and an input pin receives a voltage less than a second reference voltage.

19(Original). The method of claim 14, further comprising the step of operating in an off-operating state when a brown-out occurs that includes receiving a signal that is proportional to a line voltage that is less than a second reference voltage.

20(Original). The method of claim 14, further comprising the step of operating in an off-operating state when a black-out occurs that includes receiving a signal that is proportional to a line voltage that is less than a second reference voltage.

21(Previously Cancelled).

22(Previously Cancelled).

23(Previously Cancelled).

24(Previously Cancelled).

25(Previously Cancelled).

26(Previously Cancelled).

27(Previously Amended). A method of controlling an integrated regulator circuit in a power converter, comprising:

controlling a switching signal of the integrated regulator circuit in response to a feedback signal received externally to the integrated regulator circuit;

providing a control signal to the integrated regulator circuit which alters the switching signal of the integrated regulator circuit over multiple cycles of the switching signal wherein the control signal is received externally to the integrated regulator circuit; and

storing a mode of operation of the integrated regulator circuit in a memory circuit.

28(Previously Amended). The method of claim 27 wherein providing the control signal includes altering the switching signal of the integrated regulator circuit to disable the power converter.

29(Previously Amended). The method of claim 27 wherein providing the control signal includes altering the switching signal of the integrated regulator circuit to reduce power conversion of the power converter.

30(Previously Amended). The method of claim 27 further including:

comparing the control signal to a reference signal and generating a first signal; and

setting the mode of operation of the integrated regulator circuit according to the first signal to alter the switching signal of the integrated regulator circuit.

31(Previously Amended). The method of claim 30 further including storing a state of the first signal in the memory circuit to set the mode of operation of the integrated regulator circuit.

32(Previously Amended). An integrated circuit containing a regulator circuit, the regulator circuit comprising:

a state circuit having an input coupled for receiving a control signal from external to the regulator circuit and an output for providing a mode signal in response to the control signal;

a switching regulator circuit having a first input coupled for receiving a feedback signal, an output for providing a switching signal of the regulator circuit, and a control input coupled for receiving the mode signal; and

a memory circuit coupled to receive a state of the control signal and responsively store a mode of operation of the regulator circuit.

33(Previously Amended). The regulator circuit of claim 32, wherein the state circuit includes a comparator having a first input coupled for receiving the control signal, a second input coupled for receiving a first reference signal, and an output.

34(Previously Amended). The regulator circuit of claim 33, wherein the memory circuit includes a first input coupled to an output of the comparator for setting an output state of the memory circuit as the mode signal according to the state of the control signal.

35(Previously Amended). The regulator circuit of claim 32, wherein the memory circuit has at least one storage element for storing the mode of operation of the regulator circuit.

36(Previously Amended). The regulator circuit of claim 33, wherein the state circuit further includes a resistor divider network for generating the first reference signal at a first output and a second reference signal at a second output.

37(Previously Amended). The regulator circuit of claim 33, wherein the comparator includes:

a first comparator having a first input coupled for receiving the control signal, a second input coupled for receiving the first reference signal, and an output coupled to a first input of the memory circuit; and

a second comparator having a first input coupled for receiving the control signal, a second input coupled for receiving a second reference signal, and an output coupled to a second input of the memory circuit.

38(Previously Cancelled).

39(Previously Cancelled).

40(Previously Cancelled).

41(Previously Amended). In a power conversion system, an integrated switching regulator circuit operating in response to a feedback signal from the power conversion system for providing a switching signal to the power conversion system, the integrated switching regulator circuit comprising;

a control input coupled for receiving an operating mode control signal from external to the integrated switching regulator circuit which sets a mode of operation of the integrated switching regulator circuit; and

a memory circuit having a first input coupled to receive a state of the operating mode control signal from an output of a comparator and responsively set an output state of the memory circuit to set the mode of operation.

42(Previously Amended). The integrated switching regulator circuit of claim 41 further including a state circuit having an input coupled for receiving the operating mode control signal and an output for setting the output state of the memory circuit.

43(Previously Amended). The integrated switching regulator circuit of claim 42, wherein the comparator includes a first input coupled for receiving the operating mode control signal, a second input coupled for receiving a first reference signal, and an output coupled to the first input of the memory circuit.

44(Previously Cancelled).

45(Previously Amended). A semiconductor chip having a regulator circuit formed to provide a drive signal used to regulate power transfer of a power supply in response to a feedback signal and formed to receive an external control signal used to suspend power transfer of the power supply, the regulator circuit comprising:

a state circuit having an input coupled for receiving the external control signal and an output for providing a mode signal in response to the external control signal—wherein the state circuit includes a memory circuit having a first input coupled to an output of a comparator for setting an output state of the memory circuit as the mode signal according to a value of the external control signal; and

a switching regulator circuit having a first input coupled for receiving the feedback signal, a control input coupled for receiving the mode signal, and an output for providing the drive signal in response to the feedback signal and the mode signal.

46(Previously Amended). The semiconductor chip of claim 45, further including the comparator having a first input coupled for receiving the external control signal, a second input

coupled for receiving a first reference signal, and the output coupled to the first input of the memory circuit.

47(Previously Cancelled).

48(Previously Amended). The semiconductor chip of claim 45, wherein the memory circuit has at least one storage element for storing a mode of operation of the regulator circuit.

49(Previously Amended). The semiconductor chip of claim 46, wherein the state circuit further includes a resistor divider network for generating the first reference signal at a first output and a second reference signal at a second output.

50(Previously Amended). The semiconductor chip of claim 46, wherein the comparator includes:

a first comparator having the first input coupled for receiving the external control signal, a second input coupled for receiving the first reference signal, and the output coupled to the first input of the memory circuit; and

a second comparator having a first input coupled for receiving the external control signal, a second input coupled for receiving a second reference signal, and an output coupled to a second input of the memory circuit.

51(Previously Amended). In a power supply, an integrated circuit having a switching regulator responsive to a feedback signal from the power supply for providing a switching signal to the power supply, the switching regulator comprising a control input coupled for receiving a mode control signal from external to the integrated circuit which suspends the switching signal to the power supply; and

the integrated circuit further including a state circuit external to the switching regulator, the state circuit having a memory circuit coupled to set an output state of the memory circuit responsively to a state of the mode control signal.

52(Previously Amended). The integrated circuit of claim 51 further including the state circuit having an input coupled for receiving the mode control signal and an output for providing a mode signal in response to the mode control signal to set a mode of operation of the switching regulator.

53(Previously Amended). The integrated circuit of claim 52, wherein the state circuit includes a comparator having a first input coupled for receiving the mode control signal, a second input coupled for receiving a first reference signal, and an output coupled to an input of the memory circuit.

54(Previously Cancelled).

55(Previously Cancelled).

56(Previously Cancelled).

57(Previously Added). The semiconductor chip of claim 8 further including a memory circuit coupled to receive a state of the control signal and responsively store an operating state of the internal regulator.

58(Previously Added). The semiconductor chip of claim 8 further including a memory circuit having an input coupled to receive a first state of the control signal and responsively store a first operating state of the internal regulator and to receive a second state of the control signal and responsively store a second operating state of the internal regulator.

59(Previously Added). The semiconductor chip of claim 8 further including a comparator coupled to receive the control signal from external to the semiconductor chip and responsively set a state of the control signal in a memory circuit.

60(Previously Added). The semiconductor chip of claim 59 wherein the comparator includes a first comparator having a first input coupled to a first reference signal and an output coupled to a first input of the memory and a second comparator having a first input coupled to a second reference signal and an output coupled to a second input of the memory.